CLAIMS

What is claimed is:

1. A method of reducing duty cycle distortion in a data output signal comprising data read from a memory device, the method comprising the acts of:

providing a reference clock signal to a synchronization circuit coupled to an output data circuit configured to store the data being read from the memory device;

delaying and distorting the reference clock signal by the synchronization circuit to produce a distorted output clock signal; and

applying the distorted output clock signal to the data output circuit to remove the stored data therefrom synchronous with the reference clock signal.

2. The method as recited in claim 1, wherein the reference clock signal comprises falling edges and rising edges, and wherein, when the distorted output clock signal is applied to the data output circuit, the stored data is removed therefrom synchronous with the falling edges and the rising edges of the reference clock signal.

3. The method as recited in claim 1, wherein, when the distorted output clock signal is applied to the data output circuit, the data output circuit generates a data output signal comprising the stored data, the data output signal having reduced duty cycle distortion.

4. The method as recited in claim 3, wherein the data output signal has a 50% duty cycle.

5. The method as recited in claim 1, comprising the act of:

determining an amount of data duty cycle distortion introduced by the data output circuit; and

wherein the act of distorting the reference clock signal comprises distorting the reference clock signal in phase inverse relationship to the determined amount of duty cycle distortion.

6. The method as recited in claim 5, wherein the act of determining the amount of data duty cycle distortion comprises the act of:

providing a model of the data output circuit in a feedback path in the synchronization circuit.

7. The method as recited in claim 6, wherein the model comprises a copy of the data output circuit.

8. The method as recited in claim 7, wherein the data output circuit comprises a latch.

9. The method as recited in claim 1, wherein the reference clock signal comprises rising edges and falling edges, and wherein the act of delaying and distorting the reference clock signal comprises the acts of:

adjusting timing of the rising edges of the reference clock signal; and

adjusting timing of the falling edges of the reference clock signal.

10. The method as recited in claim 1, wherein the act of delaying and distorting the reference clock signal comprises:

delaying the reference clock signal to generate an output clock signal, wherein the output clock signal comprises rising edges and falling edges; and

distorting the output clock signal by adjusting timing of the rising edges of the output clock signal and adjusting timing of the falling edges of the output clock signal to generate the distorted output clock signal.

11. The method as recited in claim 10, comprising the acts of:

determining an amount of data duty cycle distortion introduced by the data output circuit; and

wherein the act of distorting the output clock signal comprises distorting the output clock signal in phase inverse relationship to the determined amount of duty cycle distortion.

12. A method of reading data from a synchronous memory device, comprising the acts of:

accessing data in a memory array of the synchronous memory device in response to a read request;

storing the accessed data in an output circuit;

removing the stored data as a data output signal synchronous with a reference clock signal, wherein the act of removing comprises the acts of:

providing the reference clock signal to a synchronization circuit coupled to the output circuit, the reference clock signal having a reference duty cycle; and

distorting the reference duty cycle of the reference clock signal to generate an output clock signal having a distorted duty cycle, such that, when the output clock signal is applied to the output circuit, the output circuit generates the data output signal, the data output signal having an output duty cycle that is substantially the same as the reference duty cycle.

13. The method as recited in claim 12, comprising the act of adjusting a phase of the reference clock signal to generate the output clock signal having a shifted phase relative to the phase of the reference clock signal.

14. The method as recited in claim 12, wherein the reference clock signal comprises falling edges and rising edges, and wherein the acting of distorting the reference duty cycle of the reference clock signal comprises the acts of:

adjusting timing of the rising edges; and

adjusting timing of the falling edges.

15. The method as recited in claim 14, wherein the data output signal comprises falling edges and rising edges, and wherein, when the output clock signal is applied to the output circuit, the falling edges of the data output signal are synchronous with one of the falling edges and the rising edges of the reference clock signal, and the rising edges of the data output signal are synchronous with the other one of the falling edges and the rising edges of the reference clock signal.

16. The method as recited in claim 14, wherein the act of adjusting timing of the rising edges is performed separately from the act of adjusting timing of the falling edges.

17. The method as recited in claim 12, comprising the act of:

determining an amount of data duty cycle distortion introduced by the data output circuit; and

wherein the act of distorting the reference duty cycle of the reference clock signal comprises the act of distorting the reference duty cycle in phase inverse relationship to the determined amount of data duty cycle distortion.

18. The method as recited in claim 17, wherein the act of determining an amount of data duty cycle distortion comprises the act of:

providing a model of the output circuit in a feedback path of the synchronization circuit.

19. The method as recited in claim 18, wherein the output circuit comprises a latch.

20. A processor-based device, comprising:

a timing source to provide a reference clock signal;

a processor operating synchronous with the reference clock signal; and

a synchronous memory device coupled to the processor, the synchronous memory device comprising:

a memory array to store data;

an output circuit operatively coupled to the memory array to hold data accessed from the memory array in response to a read request from the processor; and

a delay lock loop operatively coupled to the timing source and the output circuit, the delay lock loop configured to receive the reference clock signal and to generate an output clock signal based on the reference clock signal, the delay lock loop comprising:

a synchronization circuit configured to generate the output clock signal by shifting phase of the reference clock signal and adjusting a clock duty cycle of the reference clock signal, such that, when the output clock signal is applied to the output circuit, a data output signal comprising the data is generated, the data output signal being synchronous with the reference clock signal and having an output duty cycle substantially the same as the clock duty cycle.

21. The device as recited in claim 20, wherein the reference clock signal comprises falling edges and rising edges, and wherein the synchronization circuit comprises a first adjustment circuit configured to adjust timing of the falling edges, and a second adjustment circuit configured to adjust timing of the rising edges.

22. The device as recited in claim 21, wherein the synchronization circuit comprises a feedback circuit configured to provide a first feedback signal and a second feedback signal, wherein the first adjustment circuit adjusts the rising edges based on the first feedback signal, and the second adjustment circuit adjusts the falling edges based on the second feedback signal.

23. The device as recited in claim 22, wherein the feedback circuit comprises a model of the output circuit.

24. The device as recited in claim 23, wherein the output circuit comprises a latch.

25. The device as recited in claim 23, wherein the model comprises a copy of the output circuit.

26. The device as recited in claim 21, wherein the first adjustment circuit comprises a first delay line and a first phase detector, and wherein the second adjustment circuit comprises a second delay line and a second phase detector.

27. The device as recited in claim 20, wherein the output circuit introduces a duty cycle distortion in the output duty cycle of the output data signal, and wherein the synchronization circuit is configured to adjust the clock duty cycle of the reference clock signal in a phase inverse relationship to the duty cycle distortion introduced by the output circuit.

28. The device as recited in claim 27, wherein the synchronization circuit comprises a feedback circuit to generate a feedback signal, and the synchronization circuit adjusts the clock duty cycle based on the feedback signal.

29. The device as recited in claim 28, wherein the feedback circuit comprises a model of the output circuit.

30. The device as recited in claim 28, wherein the feedback circuit comprises a copy of the output circuit.

31. The device as recited in claim 20, wherein the synchronous memory device comprises a synchronous dynamic random access memory.

32. A delay lock loop, comprising:

an input configured to receive a reference clock signal having a reference duty cycle;

an output configured to couple an output clock signal to an output circuit, the output circuit configured to store data;

an adjustment circuit coupled between the input and the output, the adjustment circuit being configured to generate the output clock signal, the output clock signal being phase-shifted relative to the reference clock signal and having an output duty cycle different than the reference duty cycle,

wherein, when the output clock signal is applied to the output circuit, the output circuit generates a data output signal comprising the stored data, the data output signal being synchronous with the reference clock signal and having a data output duty cycle substantially the same as the reference duty cycle.

33. The delay lock loop as recited in claim 32, wherein the reference clock signal comprises falling edges and rising edges, wherein the output clock signal comprises output falling edges and output rising edges, and wherein the adjustment circuit comprises:

a first adjustment circuit to adjust timing of the falling edges of the reference clock signal to generate the output falling edges of the output clock signal; and

a second adjustment circuit to adjust timing of the rising edges of the reference clock signal to generate the output rising edges of the output clock signal.

34. A delay lock loop, comprising:

an input configured to receive a reference clock signal having a reference duty cycle;

an output configured to couple an output clock signal to an output circuit, the output circuit configured to store data; and

an adjustment circuit coupled between the input and the output, the adjustment circuit being configured to adjust the reference duty cycle of the reference clock signal to generate the output clock signal,

wherein, when the output clock signal is applied to the output circuit, the output circuit generates a data output signal comprising the stored data, the data

output signal being synchronous with the reference clock signal and having reduced duty cycle distortion.

35. The delay lock loop as recited in claim 34, wherein the output circuit introduces duty cycle distortion, and wherein the adjustment circuit adjusts the reference duty cycle in phase inverse relationship to the duty cycle distortion introduced by the output circuit.

36. The delay lock loop as recited in claim 35, comprising a feedback circuit coupled to the adjustment circuit, the adjustment circuit configured to adjust the reference duty cycle based on the feedback signal, wherein the feedback circuit comprises a model of the output circuit.

37. The delay lock loop as recited in claim 36, wherein the model comprises a copy of the output circuit.

38. The delay lock loop as recited in claim 34, wherein the reference clock signal comprises rising edges and falling edges, and wherein the adjustment circuit comprises a first adjustment circuit to adjust timing of the rising edges of the reference

clock signal, and a second adjustment circuit to adjust timing of the falling edges of the reference clock signal.

39. An integrated circuit, comprising:

a memory array to store data;

an input for receiving a reference clock signal;

an output circuit to store data accessed from the memory array in response to a read request; and

a synchronization circuit coupled to the input and the output circuit, the synchronization circuit configured to generate an output clock signal, such that, when the output clock signal is applied to the output circuit, the output circuit generates an output data signal comprising the data, the output data signal being synchronous with the reference clock signal and having reduced duty cycle distortion.

40. The integrated circuit as recited in claim 39, wherein the integrated circuit comprises a synchronous memory device.

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~~42~~. The integrated circuit as recited in claim 39, wherein the integrated circuit comprises a synchronous dynamic random access memory.